PROM PROGRAMMER
PROGRAM CARD SET
909 - 1917
DATA I/O

Instruction manual

DATA I/O

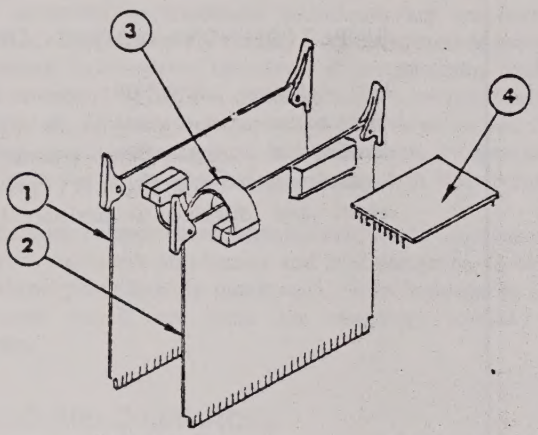
Programming systems for tomorrow...today

PROM PROGRAMMER
Program Card Set
909-1417

REV B AUG 78

025-1417

SPECIFICATION



1. Digital Card	701-1418
2. Analog Card	701-1417
3. Interconnect Cable	709-1608
4. Calib. Program Adapter	910-1417

Figure 1-1. Program Card Set 909-1417.

Table 1-1. PROM types to Data I/O Socket Adapters.

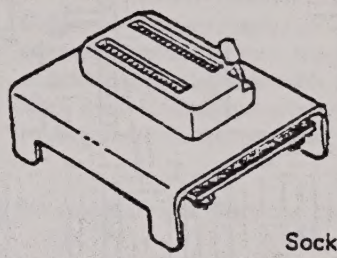
Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
INTEL				
1Kx8	8741	VOH	40 PIN	1448
1Kx8	8748	VOH	40 PIN	1448
2Kx8	8755	VOL	40 PIN	1447-1
2Kx8	8755A	VOL	40 PIN	1447-2

DESCRIPTION

Program (Personality) Card Set 909-1417 with the appropriate Socket Adapter, provides Data I/O PROM programmers with the capability of programming and reading the PROMs listed in Table 1-1. Socket Adapters are available for each PROM listed. Table 1-1 references the Socket Adapters required to program (or read) the various PROMs.

INSTALLATION

Turn power OFF while changing Card Sets. Install the Digital Card in programmer Brown-Orange card slot; install the interconnected Analog Card in White-White card slot. Component sides of cards should face forward in programmer Models 1-5, to the right in programmer satellites, and down in programmer Models 7 and 9. Connect J2 on Analog Card to front panel Socket Receptacle. Refer to the programmer manual for more detailed installation instructions.



Socket Adapter

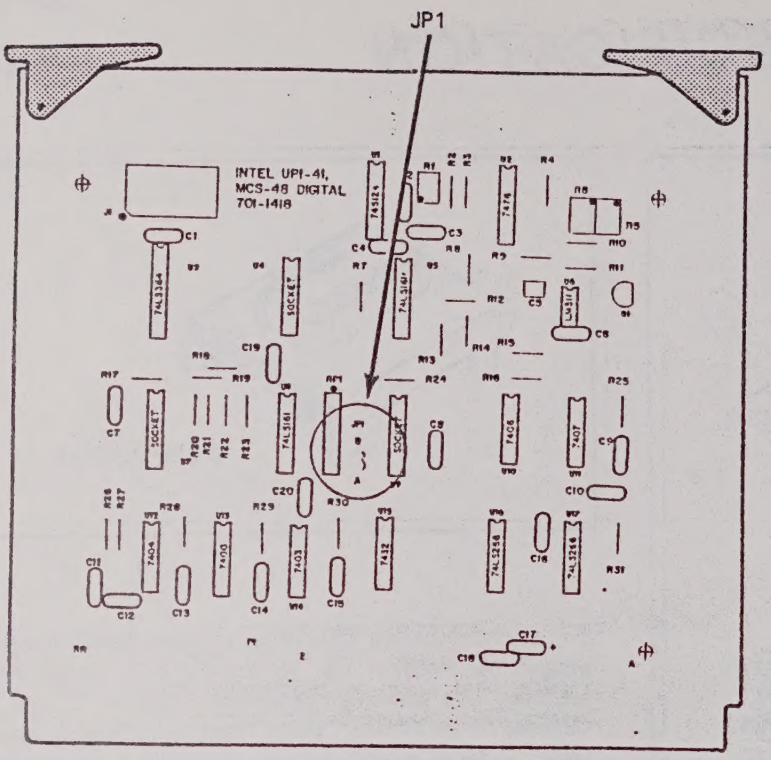
NOTE: The 909-1417 Card Set functions in all Model 1-5 programmers. Do not use the Satellite. Model 7 and 9 programmers require Revision B Control Software. If the LOAD indicator remains ON when power is applied to the Model 7 or 9 programmer, the programmer will accommodate the card set.

CALIBRATOR PROGRAM ADAPTER

Program Card Set 909-1417 includes Calibrator Program Adapter 910-1417 which mates with the Data I/O Universal Calibrator. As shipped, this Program Card Set is precalibrated according to Data I/O Calibration Procedure 017-1417 which is included in the Performance Check Section of this manual.

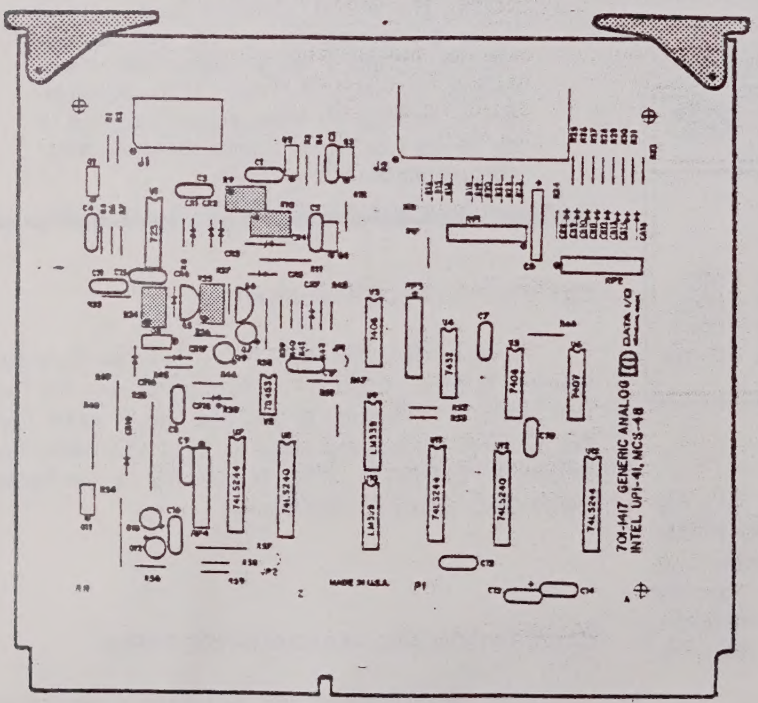
CALIBRATION AND PERFORMANCE CHECK

Card Set calibration and performance verification precedures are given in the following pages. Calibration should be performed every 90 days, or if PROM programming yields fall below PROM manufacturers' recommendations. Performance Check should be performed after each calibration.



JUMPER POSITIONS, DIGITAL CARD

JP1 — Reject jumper JP1 enables a reject to be signaled after the specified number of programming attempts. Reject is enabled in position A (1 pulse reject) and disabled in position B.



ADJUSTMENT LOCATIONS, ANALOG CARD

Adjustment locations are shown shaded. These adjustments are made during calibration, as explained in the following section.

CALIBRATION/PERFORMANCE CHECK

INTRODUCTION

Since PROM manufacturers' shipments can vary from lot to lot, slight variations in PROM programming yields are to be expected. However, each manufacturer usually specifies certain minimum PROM programming yields—provided that specific approved programming techniques are employed. Data I/O Programmers employ manufacturer-approved programming techniques: therefore, if programming yields diminish below PROM manufacturers' recommended minimums, or, if the program card set has been in use for more than ninety days since its last calibration, programmer performance should be checked as explained in this section.

The performance check includes calibration adjustments of program waveform amplitudes and includes go/no-go tests of all critical programming parameters. Also included in the performance check are tests on resistively loaded ac waveforms.

DATA I/O FIELD SERVICES

Data I/O, Inc. furnishes complete programmer repair and calibration services at regional Field Service Centers and at the Data I/O factory. Contact your local Data I/O representative for further information.

TEST EQUIPMENT REQUIRED

To perform a complete performance check, the following equipment is required:

1. Data I/O Universal Calibrator, P/N 910-1071.

2. A. Prog. 1, 2, 3, 5: Data I/O Extender Card, P/N 910-1136.
   B. Prog. 9: Data I/O Extender Fixture, P/N 910-1074.

3. Digital Voltmeter: Fluke Model 8000A, or equivalent

4. Adjustment Tool: A three-inch screwdriver

5. Dual Trace Oscilloscope: Tektronix 465, or equivalent

6. Programmers 1, 2, 3, 5 only: Data I/O 13 inch Interconnect Cable, P/N 709-1613.

7. Programmer 9 only: Data I/O Interconnect Cables, P/N 709-1613 and 709-2608.

8. Jumper wires approximately 12 inches in length.

INSTALLATION OF UNIVERSAL CALIBRATOR

The following installation procedure assumes that the Universal Calibrator is mated with the Extender Card and that Programmer power is off. On Programmers 1, 2, 3, and 5, remove the top cover to expose the card cage. To expose the card cage on the Model 9, open the access opening on the front of the chassis.

1. Remove end of 26-conductor cable from analog card. Remove both cards (analog and digital) from Programmer (or Satellite) card cage.

2. Remove end of 16 conductor cable from digital card J1.

CAUTION

Connector pins are fragile; careless connector extraction may result in bent or broken pins. Use a suitable tool--like a small screwdriver--when removing connectors from their sockets.

3. Install the extender card (with the Universal Calibrator in place).
   A. Programmers 1-5: Install the extender card into the analog card slot (white-white).
   B. Programmer 9: Install extender fixture into digital card slot (brown- orange).

4. A. Programmers 1-5: Install the analog card of the program card set into the card slot on top of the extender board. Refer to Figure 1.
   B. Programmer Model 9: Install the analog card in front card slot. Refer to Figure 2. The components should face the Calibrator.

5. A. Programmers 1-5: Install the digital card in the digital slot in the programmer.
   B. Programmer 9: Install the digital card behind the analog card on top of the extender card.

6. Making sure that cable red stripes and connector pins 1 are properly oriented, connect the analog card to the Universal Calibrator as follows:
   A. Programmers 1-5: Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Connect J2 of the analog card to J2 of the Universal Calibrator using the ribbon cable that connects the card set and the programmer.
   B. Programmer 9: Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Using the 26-connector cable supplied with the Calibrator, connect J2 of the analog card to J2 of the Calibrator.

7. Plug Calibrator Program Adapter into PROGRAM ADAPTER SOCKET on Universal Calibrator.

CAUTION

Be sure that the four-digit portions of both part numbers are identical: i.e. Analog card 701-XXXX is part of program card set 909-XXXX, which is calibrated by calibrator program adapter 910-XXXX.

8. Connect DVM ground probe to GND test point at left side of Universal Calibrator.

This completes installation of the Universal Calibrator.

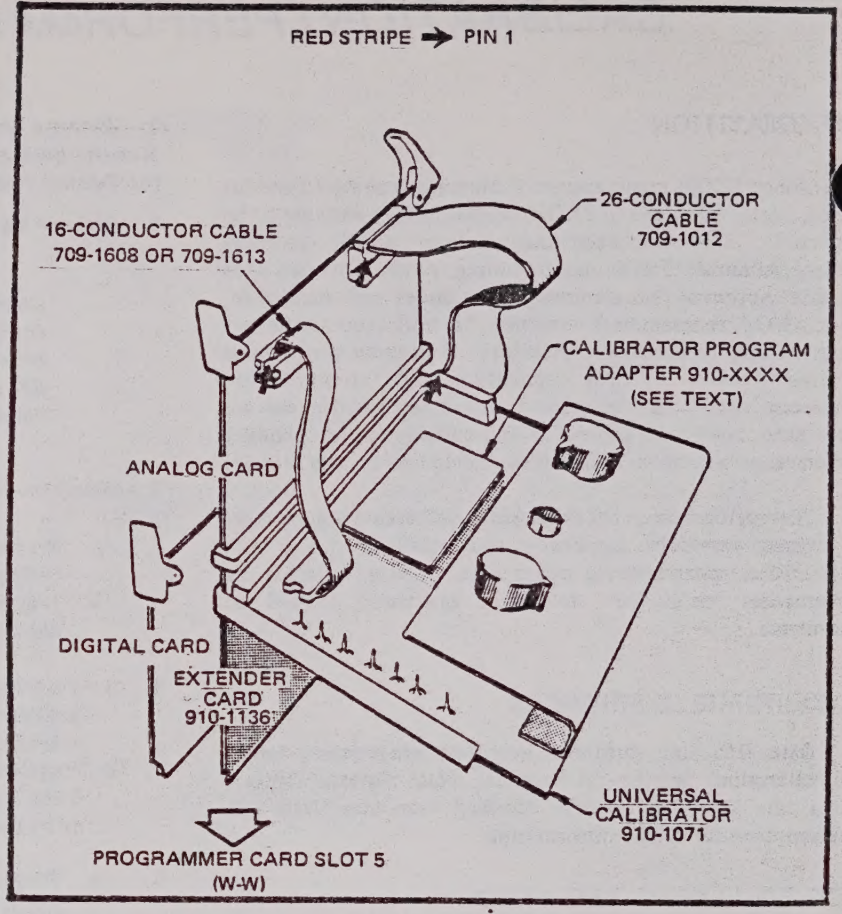


Figure 1. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for Calibration/Performance Check.

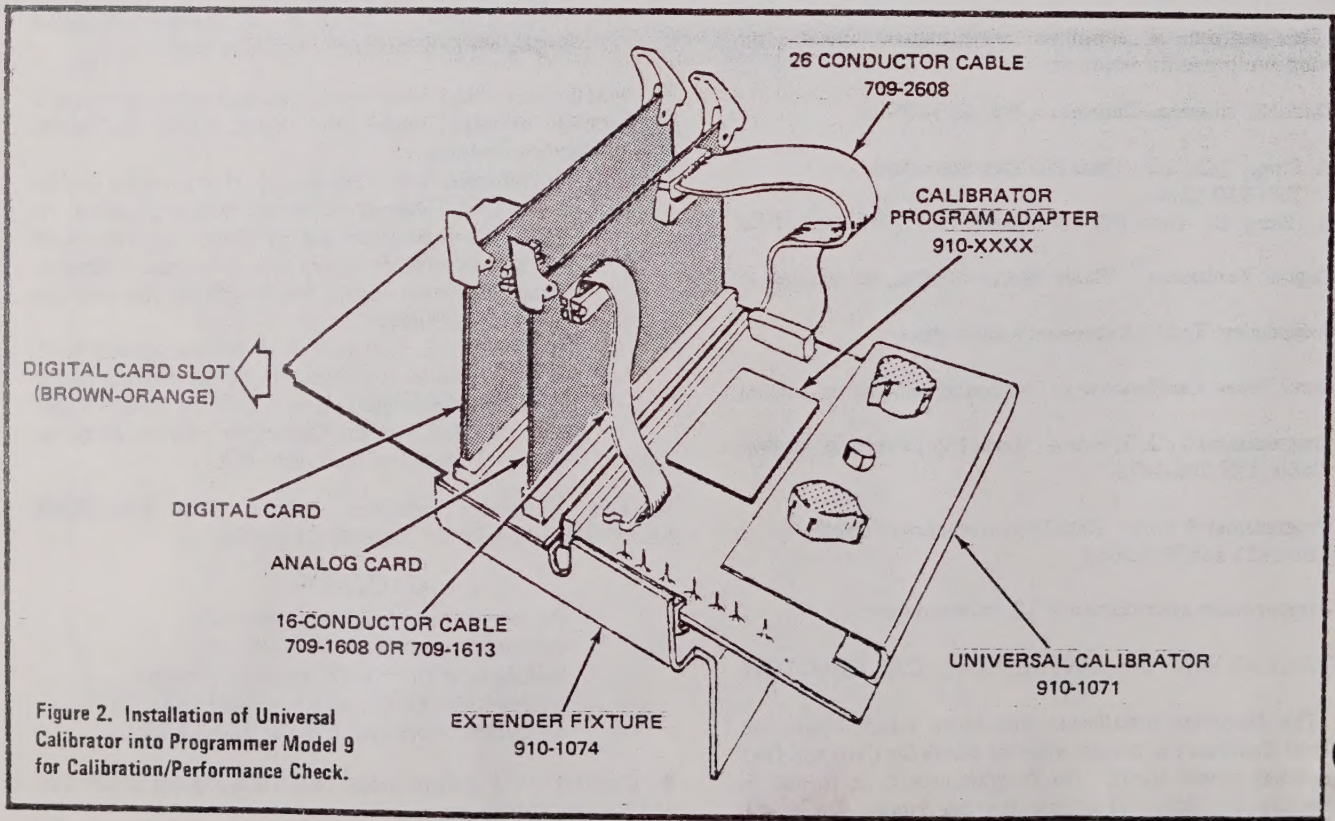


Figure 2. Installation of Universal Calibrator into Programmer Model 9 for Calibration/Performance Check.

CALIBRATION CHART

The calibration chart is to be used only with the (calibrator) program adapter specified in the title block of the chart.

The left-most portion of the chart contains truth tables for the calibrator program adapter. The truth tables are for documentation purposes only, and have no bearing on the actual performance check/calibration procedures.

PROGRAMMER WORD COUNT COLUMN is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When using the chart, refer to the address (word count) corresponding to the address readout configuration of the programmer in use. For instance, if your programmer has a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to compo-components if Programmer is left unattended with advanced word count.

TEST DESCRIPTION column contains three kinds of tests: (1) power supplies, (2) performance checks, and (3) calibration adjustments. The power supply tests are contained in the first five rows of the chart. (Note that power supply adjustments are located in the programmer, not in the program card set.) Performance checks fill the bulk of the Calibration Chart; these are characterized by min/max voltage limits only. No nominal (NOM) values are given, and no adjustments (ADJ) are prescribed.

Calibration steps are those with entries in the ADJ and NOM columns. These steps are evident by the note "CALIBRATION STEP" in the comments column.

SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load select switch; S3 is the line select switch. Generally, each step on the Calibration Chart requires changing of switch positions. S1 is push to test, and should be held depressed only long enough to obtain a DVM reading.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high Programmer current levels. Extended high current operation (S1 depressed) may damage sensitive electronic components.

TEST POINT column gives test point location for DVM probe on Universal Calibrator. Some test points are located on the program card itself; for instance, if a test point is designated as U6 P8, it means that the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the comments column.

The ADJ column calls out potientiometer designations. The first four entries in the ADJ column refer to power supply potientiometers located on the power supply board of the Programmer. If adjustments are required, refer to Programmer manual. The remaining entries in the ADJ column refer to pots on the analog card. These are located as shown on page 1-2 in the Specifications section of this manual.

The LIMITS COLUMN is divided into three portions: MIN (minimum), NOM (Nominal), and MAX (Maximum). The values given are in volts, and indicate the range into which a given DVM reading should fall when S1 is pressed. If a reading is within the limits, no adjustment is required and the programmer (or program card set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (calibration steps), the card is non functional and should not be used for programming.

NOTES are written in a block at the bottom of the calibration chart. These apply to certain calibration steps and are referenced by numbers in the comments column. Notes called out by letter in the comments column apply only to Model IX calibration.

PERFORMANCE CHECK AND CALIBRATION PROCEDURE

DC CALIBRATION

The following paragraphs describe the method by which a program card set is checked/calibrated in conjunction with the applicable Calibration Chart. The procedure assumes that the Universal Calibrator is properly installed, as previously described. The following procedure should be performed with the programmer in an ambient temperature range between 15°C to 35°C.

Initialization

1. Switch Programmer power ON; allow Programmer to warm up for approximately five minutes.
2. Programmers 1, 2, 3, and 5:
   Press: RESET
   ROM2-ROM2
   MANUAL
   PROGRAM
   START

   Programmer 9:
   Press: EXECUTE
   Set NORMAL/INVERT switch to INVERT.

Power Supply

During the procedure the programmer card cage should contain all boards normally used.

Connect DVM between GND and the Universal Calibrator test points given in Steps 1-1 through 1-5 on the Calibration Chart. Measured voltages should fall within the given limits. (Calibrator Switch positions do not matter.)

If any power supply voltage measurement reading is outside of the given range, adjustment must be made. Power supply adjustments are located on the power supply board within the Programmer.

If a Programmer Satellite is being used, check/calibrate Satellite power supply as explained in Satellite Manual.

Performance Check/Calibration

1. Use FWD and REV keys on Programmer keyboard to index the "address display" (word count) to the decimal (DEC), hexadecimal (HEX), or octal (OCT) address given in the word count column of the calibration chart.

CAUTION

DO NOT leave Word Count advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to components if Programmer is left unattended with advanced word count. Press Reset to relieve possible thermal stresses.

2. With Word Count set, and DVM probes installed between GND and the indicated test point on the universal calibrator, set switches S2 and S3 to the positions indicated. Press S1 to test.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high current levels within the Programmer. Extended high current operation (S1 depressed) puts unnecessary stress on sensitive electronic components.

3. While S1 is held, DVM readings should fall between the indicated limits for each measurement. If a DVM reading is outside of limits, or if the reading cannot be adjusted to fall within limits (ADJ column), DO NOT use the card set for programming.

Proceed through the Calibration Chart until all tests have been performed. At the conclusion of testing, turn Programmer power OFF, and proceed to AC Dynamic Tests.

AC CALIBRATION

AC Dynamic Tests

The following procedure is used to obtain the "Programmer Waveforms" shown on the Timing Diagram at the rear of this manual.

These waveforms, indicated by circled digits (①,②,③,..) on the timing diagram, are identically referenced on the Calibration Chart. The waveforms are obtained by selecting switch positions (S2 and S3) on the Universal Calibrator and feeding the selected signals to an appropriately triggered dual trace oscilloscope.

Test Set-Up

1. Make sure that programmer power is Off.

2. A. Programmers 1-5: Remove the digital card from the card cage. Refer to Figure 3.
   B. Programmer 9: Remove the digital card from the extender. Refer to Figure 4.

3. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

4. A. Programmers 1-5: Disconnect the other end of the 16-conductor cable from J1 of the analog card. Substitute the 13 inch cable supplied with the Calibrator, and connect J1 of the analog card to J1 of the digital card.
   B. Programmer 9: Connect the free end of the 16-conductor cable to digital card J1, assuring that cable red stripe and connector pin 1 are properly oriented.

5. Connect triggered input channel of dual trace oscilloscope to digital card test pulse. The location of the test pulse on the digital card is noted to the left of the Test waveform on the timing diagram. Connect the other channel to TP3 on the Calibrator. Re-install the digital card per step 2, above.

6. Using a suitable jumper cable, connect the Read Enable line emanating from analog card J1-16 to ground. (Use either the programmer chassis or the GND test point on the Universal Calibrator.)

7. Programmer 9: Set NORMAL/INVERT switch to INVERT.

CAUTION

Make sure that J1-16 is properly connected to ground. If it is inadvertently connected to any other potential, damage to Programmer components may result.

8. Turn Programmer power ON.

9. Programmers 1, 2, 3, 5:
   Press: RESET
   RAM-RAM
   PROGRAM
   MANUAL
   START
   Programmer 9:
   Press: KEYBOARD

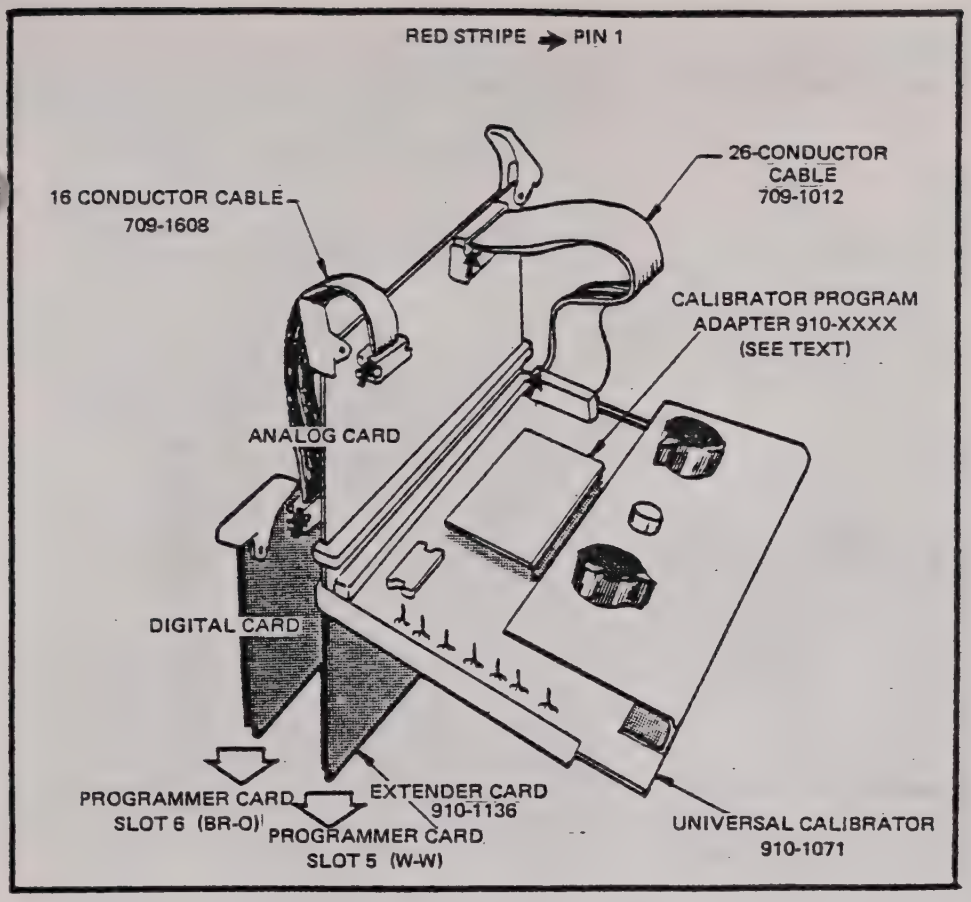


Figure 3. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for AC Dynamic Tests.

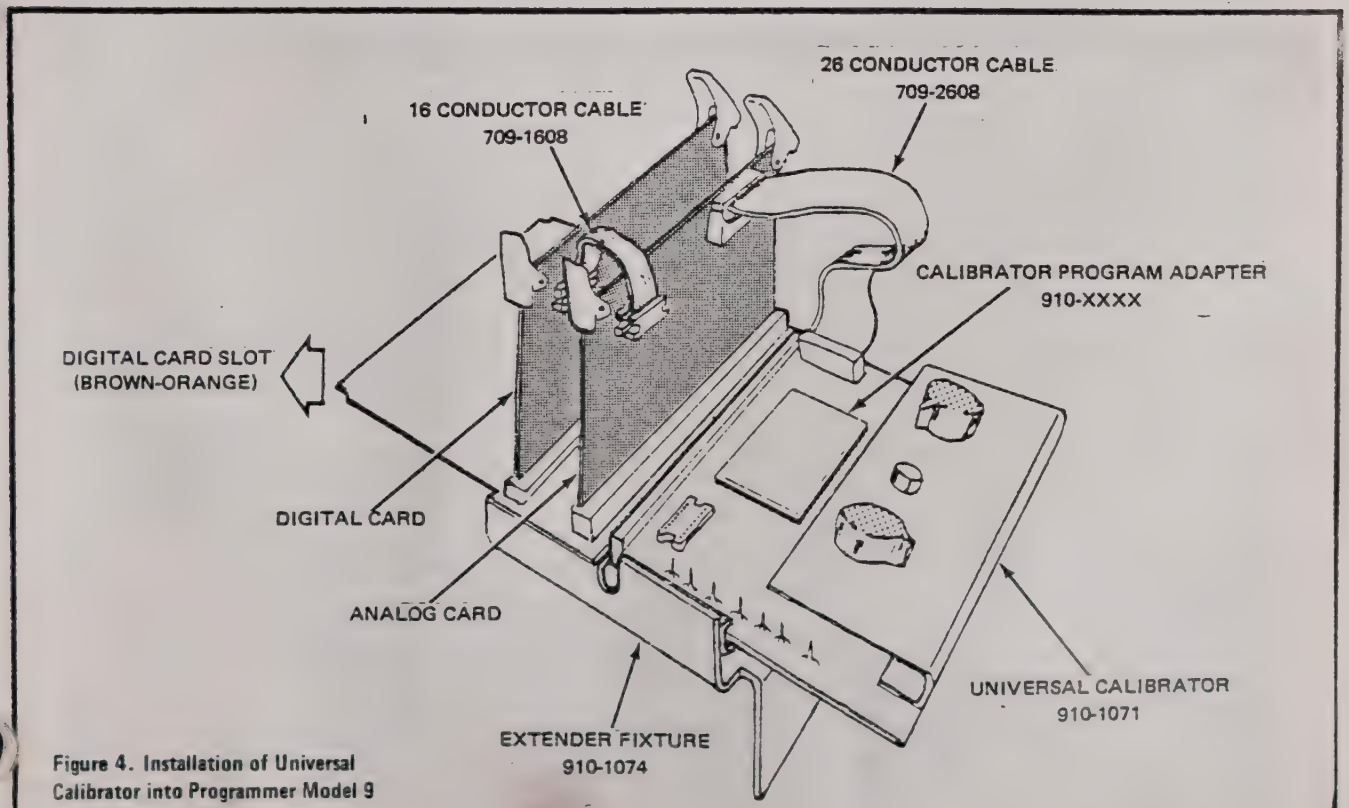


Figure 4. Installation of Universal Calibrator into Programmer Model 9 for AC Dynamic Tests.

10. Load approximately ten RAM addresses with bit 1 (only). This is accomplished by pressing 1 and FWD repetitively, or a tape may be used.

11. Programmers 1, 2, 3, 5:
Press: RESET
PROG
AUTO
RAM-ROM2

Programmer 9:
Press: PROGRAM

Waveform Observations

Initiate waveforms:
Programmers 1-5: press START.
Programmer 9: press EXECUTE.

The machine will stop on those addresses loaded in step 10 of the test set-up. If an abort condition is indicated, press WORD SKIP (SKIP on the Model 9) to advance the word count and repeat output of programming waveforms. An abort condition is indicated on Models 1, 2, 3, and 5 if the PROGRAMMING and INTERRUPT indicators come on. A Model 9 displays an abort condition by flashing the "P" indicator.

The "Program Waveforms" on the timing diagram at the rear of the manual are cross-referenced to the "Test Description" column on the Calibration Chart by circled digits (①, ②, ③,...). To obtain the various waveforms use S2 and S3 on the Universal Calibrator to select the positions indicated in the "Switch Positions" column of the calibration chart and press S1 to test. S3 routes analog card output to TP3 (oscilloscope probe); S2 selects resistive loads, which are connected to ground when S1 is pressed.

NOTE: *All other information on the calibration chart is of no importance during waveform observations.*

CAUTION

When S1 is pressed high currents are induced within the Programmer; do not hold S1 depressed for extended periods. High currents are also present when the programmer is locked into program mode with advanced word count; RESET before leaving programmer unattended during these tests.

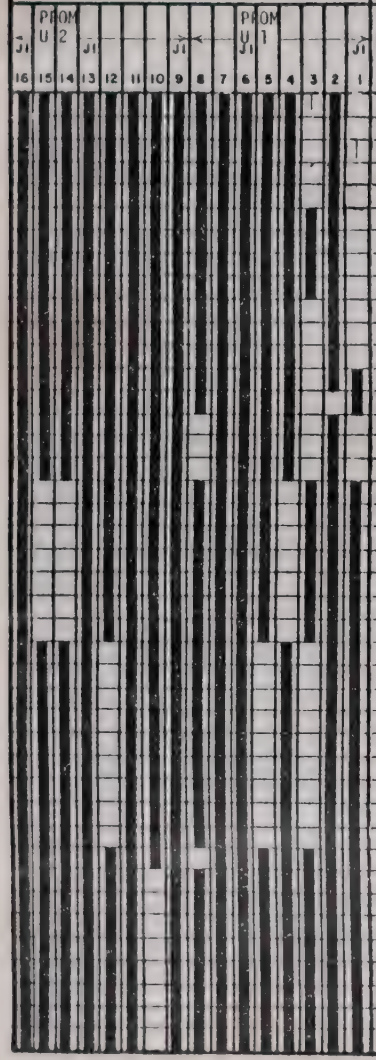
During these tests note that the Abort, Pause, and Reject functions of the program card set remain active; Press WORD SKIP to refresh the display. The abort timer signals a reject after a specific programming time. The pause timer controls the on/off time of the programming function. The position of the reject jumper (C or M) limits the number of applied programming pulses. Refer to the notes column of the timing diagram for definitions of the abort, pause, and reject functions.

DATA I/O
HEADQUAR, WASH.

CALIBRATION CHART 017-1417
FIXTURE 702-1071
PROGRAM ADAPTER 910-1417
PROGRAM CARD 909-1417

MANUFACTURE Intel
PROM 8741, 8748, 8755, 8755A

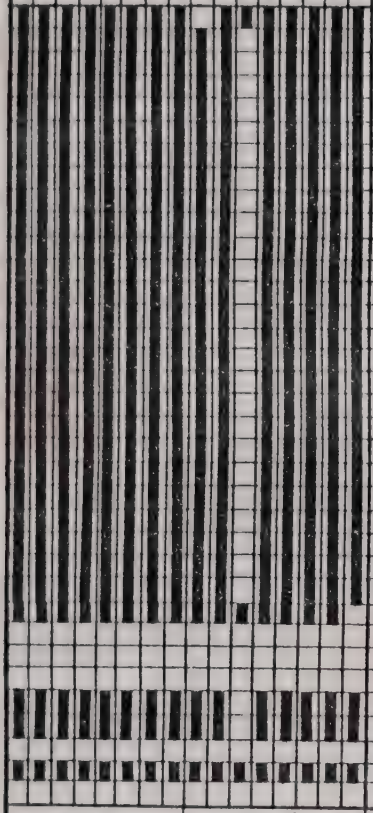
DATE	SYM	REVISION RECORD	DR	CK
5-2-73	A	RELEASE	GJ	GS
8-25-75	B	CN* 2407	K	



STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	PRESS S1	COMMENTS
													FOR MODEL V SEE NUMBERED NOTES ONLY. FOR MODEL IX SEE NUMBERED AND LETTERED NOTES.
1-1	000	00	000	+ 24			+24	R26	23.5	24.0	24.5		
1-2	000	00	000	POWER + 48			+48	R24	49.4	49.7	49.8		
1-3	000	00	000	SUPPLY + 5			+ 5	R18	5.05	5.1	5.15		
1-4	000	00	000	- 9			- 9	R40	-8.8	-9.0	-9.2		
1-5	000	00	000	PROGRAMMABLE SUPPLY			PROG V		30.0		33.0		
2-1	001	01	001	VCC PROGRAM, VERIFY (1)	5	1	TP3	R34	4.8	5.0	5.2		CALIBRATION STEP
2-2	001	01	001	VCC CURRENT LIMIT, RESET	6	1							PROGRAMMER WILL STOP. SEE NOTE A.
3-1	001	01	001	VEA HIGH (2)	2	23	TP3	R35	22.5	23.0	23.5		CALIBRATION STEP.
4-1	001	01	001	VDD VERIFY (3)	4	21	TP3	R9	4.8	5.0	5.2		CALIBRATION STEP)
4-2	002	02	002	VDD PROGRAM	4	21	TP3	R10	24.1	24.3	24.5		CALIBRATION STEP)
5-1	003	03	003	PROG/VDD HIGH (4)	4	6	TP3		24.0		24.5		
5-2	003	03	003	VDD,PROG/VDD LIMIT, RESET	5	21							PROGRAMMER WILL STOP. SEE NOTE A.
5-3	004	04	004	PROG/VDD FLOAT	10	6	TP3		5.0		5.2		
5-4	005	05	005	PROG/VDD LOW	10	6	TP3		0.0		0.2		
6-1	006	06	006	VDD KILL	2	21	TP3		0.0		1.0		
6-2	006	06	006	VCC KILL	2	1	TP3		0.0		0.5		
7-1	006	06	006	VEA LOW	2	23	TP3		0.0		1.0		
8-1	007	07	007	TØ HIGH (5)	7	9	TP3		5.0		5.2		
8-2	007	07	007	RD LOW (6)	7	8	TP3		0.0		0.2		
8-3	007	07	007	PROG/CE LOW (7)	7	7	TP3		0.0		0.2		
8-4	007	07	007	RESET/ALE LOW (8)	7	10	TP3		0.0		0.2		
8-5	007	07	007	XTAL 1 HIGH	4	12	TP3		2.0		2.45		
8-6	007	07	007	CONFIGURE 1 LOW			J1-14				0.2		TEST POINT LOCATED ON ANALOG CARD.
8-7	007	07	007	CONFIGURE 2 LOW	10	22	TP3		0.0		0.2		
8-8	008	08	010	TØ LOW	7	9	TP3		0.0		0.2		
8-9	008	08	010	$\overline{RD}$ HIGH	7	8	TP3		5.0		5.2		
8-10	008	08	010	PROG/CE HIGH	7	7	TP3		5.0		5.2		
8-11	008	08	010	RESET/ALE HIGH	7	10	TP3		5.0		5.2		
8-12	008	08	010	XTAL 1 LOW (9)	7	12	TP3		0.0		0.4		
8-13	008	08	010	CONFIGURE 1 HIGH			J1-14		5.0		5.2		TEST POINT LOCATED ON ANALOG CARD.
8-14	008	08	010	CONFIGURE 2 HIGH	10	22	TP3		5.0		5.2		
8-15	008	08	010	PULL-UP TEST	2	5	TP3		2.35		2.70		
9-1	008	08	010	COMPARATOR REF. LOW	2	5	R51		1.9		2.2		) TEST POINT: BOTTOM OF R51 ON ANALOG CARD.
9-2	009	09	011	COMPARATOR REF. HIGH	2	5	R51		2.35		2.70		)
													(SEE NOTE B FOR BELOW)
10-1	011	0B	013	BIT 8 COMPARATOR	3	13							BIT 8 LED ON,OTHER LEDS OFF(HEX 80 PROG.9 ONLY)
10-2	011	0B	013	BIT 7 COMPARATOR	3	14							BIT 7 LED ON,OTHER LEDS OFF(HEX 40 " " ")
10-3	011	0B	013	BIT 6 COMPARATOR	3	15							BIT 6 LED ON,OTHER LEDS OFF(HEX 20 " " ")
10-4	011	0B	013	BIT 5 COMPARATOR	3	16							BIT 5 LED ON,OTHER LEDS OFF(HEX 10 " " ")
10-5	011	0B	013	BIT 4 COMPARATOR	3	17							BIT 4 LED ON,OTHER LEDS OFF(HEX 08 " " ")
10-6	011	0B	013	BIT 3 COMPARATOR	3	18							BIT 3 LED ON,OTHER LEDS OFF(HEX 04 " " ")
10-7	011	0B	013	BIT 2 COMPARATOR	3	19							BIT 2 LED ON,OTHER LEDS OFF(HEX 02 " " ")
10-8	011	0B	013	BIT 1 COMPARATOR	3	20							BIT 1 LED ON,OTHER LEDS OFF(HEX 01 " " ")

STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT Press S1 TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	CALIBRATION CHART 017-1417 (CONTINUED) PAGE 2 OF 4 COMMENTS
11-1	012	00C	014	VOL DATA BIT 8 VIL	7	13	TP3		0.0		0.2	
11-2	012	00C	014	VOL DATA BIT 7 VIH	7	14	TP3		5.0		5.2	
11-3	012	00C	014	VOL DATA BIT 6 VIL	7	15	TP3		0.0		0.2	
11-4	012	00C	014	VOL DATA BIT 5 VIH	7	16	TP3		5.0		5.2	LOAD BITS 2,4,6,8(HEX AA)INPUT,LOAD HEX 55 FOR P9 ONLY)
11-5	012	00C	014	VOL DATA BIT 4 VIL	7	17	TP3		0.0		0.2	OBSERVE BITS 2,4,6,8(HEX 55 P9 ONLY)
11-6	012	00C	014	VOL DATA BIT 3 VIH	7	18	TP3		5.0		5.2	
11-7	012	00C	014	VOL DATA BIT 2 VIL	7	19	TP3		0.0		0.2	SEE NOTES 1, B AND D.
11-8	012	00C	014	VOL DATA BIT 1 VIH (10)	7	20	TP3		5.0		5.2	
11-9	013	00D	015	VOH DATA BIT 8 VIH	7	13	TP3		5.0		5.2	
11-10	013	00D	015	VOH DATA BIT 7 VIL	7	14	TP3		0.0		0.2	OBSERVE BITS 2,4,6,8(HEX 55 P9 ONLY)
11-11	013	00D	015	VOH DATA BIT 6 VIH	7	15	TP3		5.0		5.2	SEE NOTES 1 AND B.
11-12	013	00D	015	VOH DATA BIT 5 VIL	7	16	TP3		0.0		0.2	
11-13	013	00D	015	VOH DATA BIT 4 VIH	7	17	TP3		5.0		5.2	
11-14	013	00D	015	VOH DATA BIT 3 VIL	7	18	TP3		0.0		0.2	
11-15	013	00D	015	VOH DATA BIT 2 VIH	7	19	TP3		5.0		5.2	
11-16	013	00D	015	VOH DATA BIT 1 VIL	7	20	TP3		0.0		0.2	
11-17	013	00D	015	VOH DATA BIT 8 VIL	7	13	TP3		0.0		0.2	
11-18	013	00D	015	VOH DATA BIT 7 VIH	7	14	TP3		5.0		5.2	LOAD BITS 1,3,5,7(HEX 55)INPUT,LOAD HEX 55 P9 ONLY)
11-19	013	00D	015	VOH DATA BIT 6 VIL	7	15	TP3		0.0		0.2	OBSERVE BITS 1,3,5,7 (HEX 55 P9 ONLY)
11-20	013	00D	015	VOH DATA BIT 5 VIH	7	16	TP3		5.0		5.2	SEE NOTES 1, B AND D.
11-21	013	00D	015	VOH DATA BIT 4 VIL	7	17	TP3		0.0		0.2	
11-22	013	00D	015	VOH DATA BIT 3 VIH	7	18	TP3		5.0		5.2	
11-23	013	00D	015	VOH DATA BIT 2 VIL	7	19	TP3		0.0		0.2	
11-24	013	00D	015	VOH DATA BIT 1 VIH	7	20	TP3		5.0		5.2	
11-25	014	00E	016	VOL DATA BIT 8 VIH	7	13	TP3		5.0		5.2	
11-26	014	00E	016	VOL DATA BIT 7 VIL	7	14	TP3		0.0		0.2	
11-27	014	00E	016	VOL DATA BIT 6 VIH	7	15	TP3		5.0		5.2	OBSERVE BITS 1,3,5,7(HEX 55 P9)
11-28	014	00E	016	VOL DATA BIT 5 VIL	7	16	TP3		0.0		0.2	SEE NOTES 1 AND B.
11-29	014	00E	016	VOL DATA BIT 4 VIH	7	17	TP3		5.0		5.2	
11-30	014	00E	016	VOL DATA BIT 3 VIL	7	18	TP3		0.0		0.2	
11-31	014	00E	016	VOL DATA BIT 2 VIH	7	19	TP3		5.0		5.2	
11-32	014	00E	016	VOL DATA BIT 1 VIL	7	20	TP3		0.0		0.2	
12-1	015	00F	017	DATA DISABLE								LOAD ALL BITS(HEX FF)INPUT,LOAD HEX 00 P9 ONLY) OBSERVE ALL BITS OFF AT OUTPUT LED DISPLAY (SEE NOTES 1, B AND D) (HEX 00 P9).

PROM U2 TRUTH TABLE	PROM U1 TRUTH TABLE
LINE = HI (1),	NO LINE=LOW (0)



STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT PRESS S1 TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	CALIBRATION CHART 017-1417 (CONTINUED) PAGE 3 OF 4 COMMENTS
13-1	017	011	021	BACKWARDS DEVICE TEST	3	20						SEE NOTES 3 AND C.
14-1	1365	555	2525	ADDRESS TEST VIH	7	20	TP3		5.0		5.2	
14-2	1365	555	2525	ADDRESS TEST VIL	7	19	TP3		0.0		0.2	
14-3	1365	555	2525	ADDRESS TEST VIH	7	18	TP3		5.0		5.2	
14-4	1365	555	2525	ADDRESS TEST VIL	7	17	TP3		0.0		0.2	
14-5	1365	555	2525	ADDRESS TEST VIH	7	16	TP3		5.0		5.2	
14-6	1365	555	2525	ADDRESS TEST VIL	7	15	TP3		0.0		0.2	
14-7	1365	555	2525	ADDRESS TEST VIH	7	14	TP3		5.0		5.2	
14-8	1365	555	2525	ADDRESS TEST VIL	7	13	TP3		0.0		0.2	
14-9	1365	555	2525	ADDRESS TEST VIH (11)	7	2	TP3		5.0		5.2	
14-10	1365	555	2525	ADDRESS TEST VIL	7	3	TP3		0.0		0.2	
14-11	1365	555	2525	ADDRESS TEST VIH	7	4	TP3		5.0		5.2	
14-12	1365	555	2525	ADDRESS TEST VIL	7	11	TP3		0.0		0.2	SEE NOTE 2.
14-13	2730	AAA	5252	ADDRESS TEST VIL	7	20	TP3		0.0		0.2	
14-14	2730	AAA	5252	ADDRESS TEST VIH	7	19	TP3		5.0		5.2	
14-15	2730	AAA	5252	ADDRESS TEST VIL	7	18	TP3		0.0		0.2	
14-16	2730	AAA	5252	ADDRESS TEST VIH	7	17	TP3		5.0		5.2	
14-17	2730	AAA	5252	ADDRESS TEST VIL	7	16	TP3		0.0		0.2	
14-18	2730	AAA	5252	ADDRESS TEST VIH	7	15	TP3		5.0		5.2	
14-19	2730	AAA	5252	ADDRESS TEST VIL	7	14	TP3		0.0		0.2	
14-20	2730	AAA	5252	ADDRESS TEST VIH	7	13	TP3		5.0		5.2	
14-21	2730	AAA	5252	ADDRESS TEST VIL	7	2	TP3		0.0		0.2	
14-22	2730	AAA	5252	ADDRESS TEST VIH	7	3	TP3		5.0		5.2	
14-23	2730	AAA	5252	ADDRESS TEST VIL	7	4	TP3		0.0		0.2	
14-24	2730	AAA	5252	ADDRESS TEST VIH	7	11	TP3		3.0		5.2	
15-1	2730	AAA	5252	VSS TEST	8	24	TP3		0.00		0.08	
16-1	001	01	001	VEA LIMIT	3	23	TP3		7.0		10.0	
	010	0A	012									
	021	15	025									
ALL WORDS NOT SHOWN												

PROM U2 TRUTH TABLE	PROM U1 TRUTH TABLE
LINE = HI (1),	NO LINE=LOW(0)

NOTE:

1. OBSERVE OUTPUT BUSS LED DISPLAY ON PROGRAMMER FRONT PANEL. WHEN USING PROGRAMMER MODEL 9, PRESS PROM KEY FOR OUTPUT DISPLAY. S1 ON CALIBRATOR NOT DEPRESSED TO OBSERVE OUTPUT DISPLAY.
2. PROGRAMMER WORD COUNT AT STEPS 14-13 TO 14-24 IS VALID FOR PROGRAMMER 9 AND EXPANDED (4K) PROGRAMMER 5 ONLY. WHEN USING PROGRAMMER 5 WITH 2K ADDRESS LIMIT, USE 682(DEC.), 2AA(HEX) OR 1252 (OCT) FOR PROGRAMMER WORD COUNT AT STEPS 14-13 THRU 14-24,AND OMIT TEST STEPS 14-12 AND 14-24.
3. (FOR PROGRAMMER 9, SEE NOTE C). PRESS STOP. PRESS S1 AND HOLD WHILE PRESSING START. PROGRAMMER SHOULD RESET (WORD COUNT = 0) AND REMAIN IN STOP.

* FOR MODEL V SEE NUMBERED NOTES ONLY. FOR MODEL IX SEE NUMBERED AND LETTERED NOTES ON ATTACHED NOTES PAGE.

NOTES FOR

MODEL IX CALIBRATION OF 701-1417

WITH SOFTWARE 010-5900 REV. B OR LATER

Note A:

To verify Stop condition, press PROM key, observe output display; should be blank. To resume testing, press Set.

Note B:

To observe output buss LED display, press PROM key.

Note C:

To perform test press LOAD (LOAD light on). Press LOAD again (LOAD light off). Press S1 on calibrator and hold while pressing EXECUTE. Release S1 and release EXECUTE. Programmer must remain in Stop. To verify Stop condition, see Note A. This test may be performed on any programmer word count.

Note D:

To perform test:

Clear RAM: Set Normal/Invert switch to Normal, press EDIT and hold while pressing LOAD. Release LOAD, then release EDIT.

a. Select KEYBOARD
b. Set address as called out on calibration chart
c. Enter data as called out on calibration chart
d. Depress EXECUTE
e. Hold SET and press FWD
f. Depress REV key to return to address called out on calibration chart.

PROGRAM CARD SET DESCRIPTION

PROGRAM ALGORITHM

The card set begins the program operation with a backwards device test. If the device is mis-socketed, the programmer stops. Otherwise, it proceeds to the program and verify cycles.

The card set activates the program mode and applies an address to the device. It then tests for a bit to program and, if necessary, applies the program data along with a program pulse. Each address is programmed completely before the card set moves on to the next address.

PROGRAM CARD SET CIRCUIT DESCRIPTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 4-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses for the analog card until either ABORT or REJECT is signaled, or until the bit is programmed.

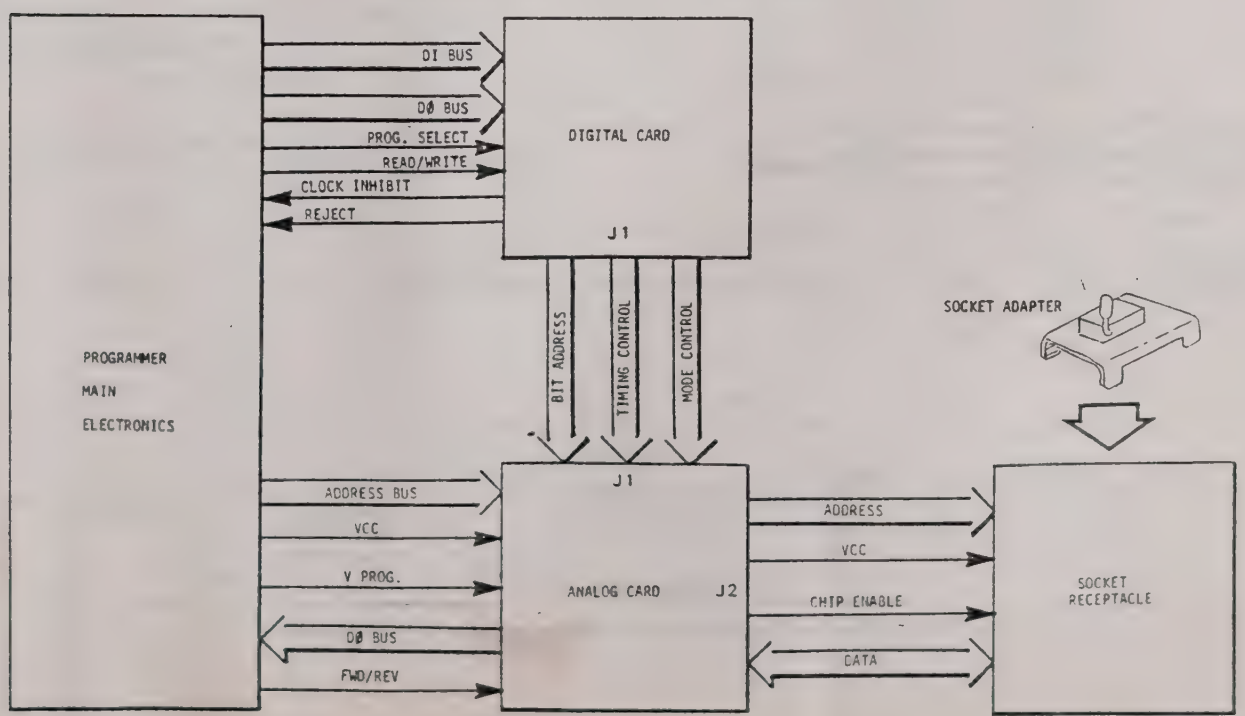
ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturer's specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow and timing. ROM truth tables, timing diagrams, jumper positions, and reject conditions are discussed. Detailed circuit schematics with timing diagrams and truth tables are found at the rear of this manual—refer to these for pin-out and interconnect information.

Figure 4.1. Simplified Block Diagram of Program Card Set.



DIGITAL CARD CIRCUIT DESCRIPTION

BLOCK DIAGRAM

The digital card block diagram is shown in Figure 4-2. The digital card receives control signals from the programmer bus shown in the diagram on the left side and outputs control signals to the analog card on the right.

SELECT AND CONTROL GATING

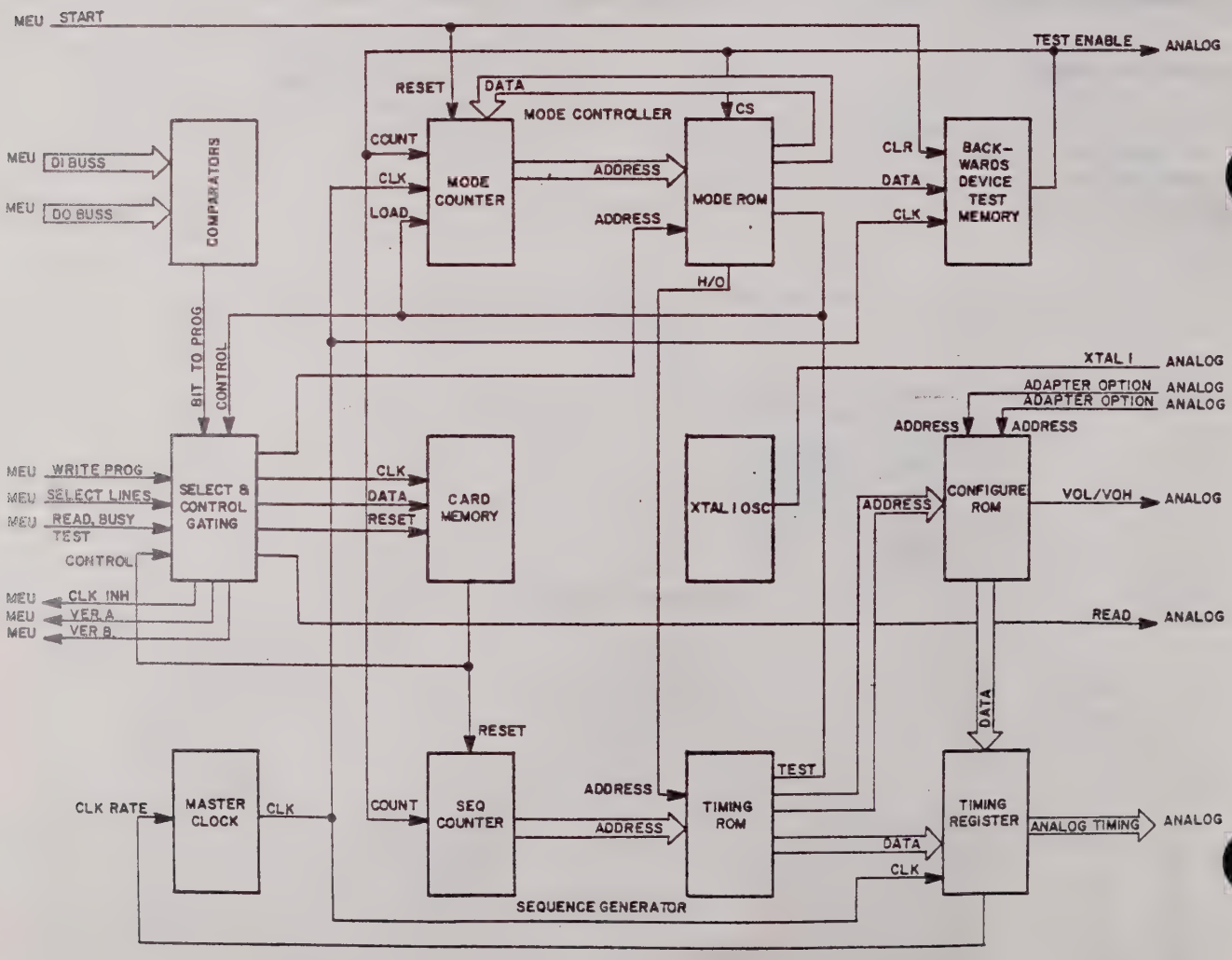
The select and control gates monitor the programmer status lines in order to enable operation of the digital card. Outputs supply data to the card memory, control the VFY A and VFY B lines for selecting 4/8 bit operation and announcing an abort condition, feed to the controller mode ROM, and control CLK INH (MEU Pin Y) to halt the programmer.

The analog card receives a signal from these gates that enables the analog card data bus drivers to output to the programmer Do bus.

CARD MEMORY

This memory serves as the interface ("handshake") control of the card set to the programmer main electronics. When the card set is selected for operation, the card memory sets upon either a Write, Read or Busy Test Pulse. This causes the digital card to begin operation and halts the programmer. Before the card memory sets, the sequence counter and backwards device memory are held reset.

Figure 4-2. Block Diagram—Digital Card, 909-1417.



MASTER CLOCK

The two-speed clock is free-running with its rate controlled by the clock rate line of the sequence generator. The slower clock rate is enabled during the program pulse time (TPW) and the faster clock rate during verify and test times. Parrallel timing is used such that all counters and memories (except the program memory) receive the same clock pulse.

BACKWARDS DEVICE TEST MEMORY

To prevent damage to a mis-socketed device, a backwards device test is performed before power is applied to the device. The backwards device test memory, when not set, enables the backwards device test to be performed. On Start, the mode controller advances until a mode counter carry is output. This carry sets the backwards device memory. Before this memory sets, and while the controller is running, a backwards device will pull reset. Once this memory is set, backwards device testing is disabled and power is applied to the device.

MODE CONTROLLER

The mode controller consists of a 4-bit (mode) counter and control ROM. When the card memory sets, the sequence counter advances to Test, enabling the controller. The controller provides digital card control during verify and program operations. The controller sends the highest order (H/O) address input to the timing ROM. This input is held low during verify and read operations and high during program.

COMPARATORS

The comparators compare the programmer DO and DI busses. When the DI and DO busses do not compare, a bit program signal is output to the control gates. This signal is fed to the controller mode ROM, enabling program operation.

SEQUENCE GENERATOR

The sequence generator includes a 4-bit (sequence) counter and a timing ROM. Addresses for the timing ROM are supplied by the sequence counter. Sequence counter operations are initiated by the master clock. The backwards device memory enables the sequence counter for loading, and the mode controller enables it for counting.

The timing ROM outputs signals that control the analog card, thereby producing waveforms as shown on the timing diagram. The timing register synchronizes these PROM outputs such at no glitches are presented to the analog card. Three of the timing ROM outputs are fed through the configure PROM and from this PROM to the timing register. The configure PROM adapts these three timing signals to the requirements of the part being programmed. One output of the configure PROM is a VOL/VOH control line to the analog card.

XTAL 1 OSCILLATOR

This oscillator provides the external timing source for the clock input on the processor parts and is asynchronous to the digital card clock. Its rate is set to a minimum of two times that of the fast rate of the digital clock. This rate ensures sufficient delays (TD) as called out on the Timing Diagram.

ANALOG CARD CIRCUIT DESCRIPTION

BLOCK DIAGRAM

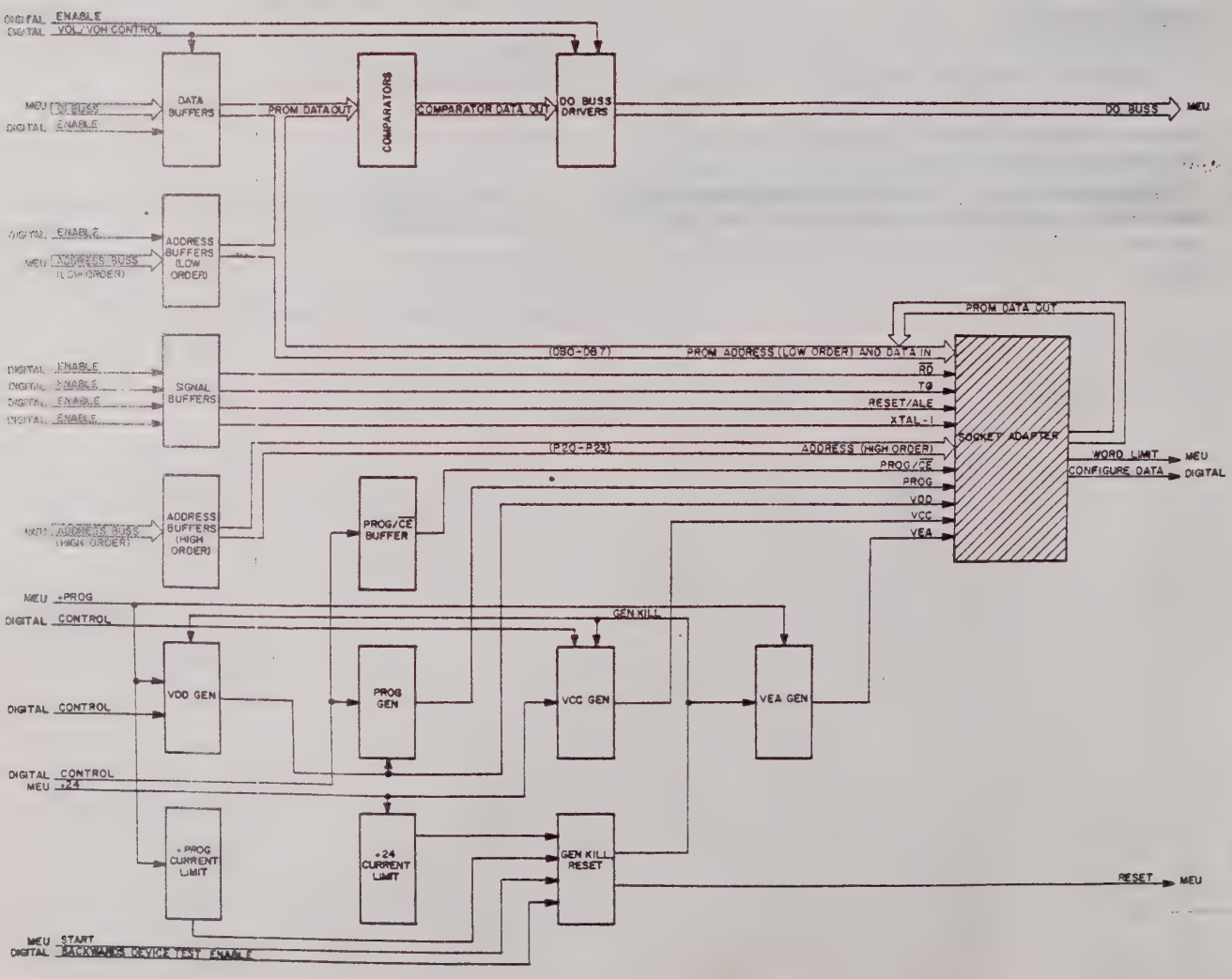
Figure 4-3 gives a generalized block diagram of the analog card. This diagram shows signal flow and functional relationships between the blocks, but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) at the rear of this manual for details of curcuit connection and operation. The following paragraphs discuss the functions contained on the analog card.

ADDRESS BUFFERS

Address buffers accommodate the eleven incoming address lines from the programmer MEU. The eight low order address lines are buffered by non-inverting gates with three state outputs. These outputs are multiplexed with the outputs of the data buffers and with the data lines of the device under program. The low order buffers have an enable input to allow them to present address to the devices. When disabled, it forces their outputs into the high impedance state.

The three high order address buffers are non-inverting gates with uncommitted collector outputs. These outputs have resistor pull-ups to +5 volts, and tie to a separate port.

Figure 4-3. Block Diagram—Analog Card, 909-1417.



DATA BUFFERS

Data buffers accommodate the eight incoming DI bus lines from the programmer MEU. These buffers are either inverting or non-inverting, as selected by the socket adapter via the digital card configure PROM. For VOL devices, the buffers are selected as non-inverters and for VOH devices as inverters. When enabled, the data buffers output data to be programmed to the device under program.

COMPARATOR AND DO BUS DRIVERS

The comparator compares programmed data against a reference level. During read, comparator outputs are transferred to the DO Bus drivers. This transfer allows the digital card to compare the device output (DO Bus) and the programmer DI Bus. The DO Bus drivers are selected as inverters or non-inverters by the same means used by the Data Buffers.

SIGNAL BUFFERS

These buffers output the specified timing signals — RD, T0, Reset, ALE and XTAL-1—to the device during program and verify operations. The buffers are inverting or non-inverting gates with uncommitted collector outputs. These outputs have resistor pull-ups to either the device VCC or +5 volts.

VDD GENERATOR

The VDD Generator is a current limited regulator with three selectable states. The VDD program statis is selected while programming pulses are being applied to the device. The VDD verify state is selected during verify and read operations. When the programmer is in Stop or Backwards Device Test, the generator is held to a zero voltage state. These levels are selected by signals from the digital card and may ba adjusted using potentiometers R1 and R2.

PROGRAM GENERATOR

The Program Generator supplies the specified program voltage to the PROG. or VDD pin of the device under program. The generator has three selectable states: active pull-up to the VDD generator, active pull-down to ground, and high impedance (float) state. These levels are selected by signals from the digital card.

VCC GENERATOR

The VCC Generator is a two-state regulator that supplies the required voltage to the VCC pin of the device. The generator is an adjustable shunt regulator with an emitter follower. During programmer stop and backwards device test conditions, its output is held to zero volts. During program and read its output is set to the specified value. This value is adjustable using potentiometer R3.

VEA GENERATOR

The VEA Generator is a two-state regulator that supplies the specified VEA voltage to the device. During stop and backwards device test conditions, the generator output is held to zero volts. During program and read, its output is set to the specified VEA voltage. The generator is an adjustable shunt regulator controlled by potentiometer R4.

PROGRAM CE/BUFFER

This buffer outputs the specified Program/CE signal to the part during verify and program. The buffer is an inverting gate with uncommitted collector output a resistor pull-up to +5 volts.

The timing enable signal for this buffer is the same as for the VDD generator.

CURRENT LIMIT AND RESET CIRCUITS

The VDD, VCC and VEA generators have foldback current limiting. When the current limit of either supply is reached, reset is pulled and the supply is shut down. Once reset is pulled, stop is held and keeps all supplies shut off.

Warranty

Data I/O equipment is guaranteed against defects in materials and workmanship. The warranty period is ninety days on new equipment, and thirty days on used equipment. Warranty period begins on receipt of equipment. Data I/O will repair or replace, at Data I/O/s option, any equipment found to be defective within the warranty period.

Warranty service will be provided by Data I/O within a reasonable amount of time after notification by the purchaser to Data I/O of equipment malfunction. This service shall not apply to equipment that has been subjected to abuse, misuse, negligence or accident as determined by Data I/O, or to which any modifications, alterations, or attachments have been made without written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in an environment containing excessive dirt, dust, moisture, fumes, humidity, or extremes of temperature.

This warranty policy is in lieu of all other warranties, expressed or implied, unless standard warranty exceptions are granted by Data I/O in writing.

Service

After expiration of the warranty period, service and repairs are billed at standard hourly rates, plus expenses, portal-to-portal. Time and one-half rate will apply outside of normal working hours.

Cost of engineering (where applicable) and parts, plus the cost of installation is billed at standard service labor rates when implementing approved, customer requested modifications.

Shipment

Products returned to Data I/O should be accompanied by a letter or enclosure explaining the reason for their return and action requested of Data I/O. Please include the following additional information: Company name and address; attention of; method of shipment desired; serial number; date of purchase; billing information, and purchase order number.

All products returned to Data I/O must be sent prepaid F.O.B. The warranty is voided if returned items are not packaged by the customer in original packing material, or in other Data I/O approved containers. If reshipment method is not specified by customer, Data I/O will return products by most expedient shipping method, F.O.B. our plant.

Ship returned equipment to:

DATA I/O CORPORATION
1297 N.W. Mall
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

Parts Ordering

Orders for parts should contain the following information:

a. Description of part(s) and Data I/O part number(s).
b. Quantity of each item to be ordered.
c. Equipment serial number and model number.
d. Corporate name of firm.
e. Shipping address of firm, including zip code.
f. Full name of person ordering the part(s).
g. To whose attention the part(s) are to be shipped.
h. Billing information.
i. Purchase order number.
j. Method of shipment.

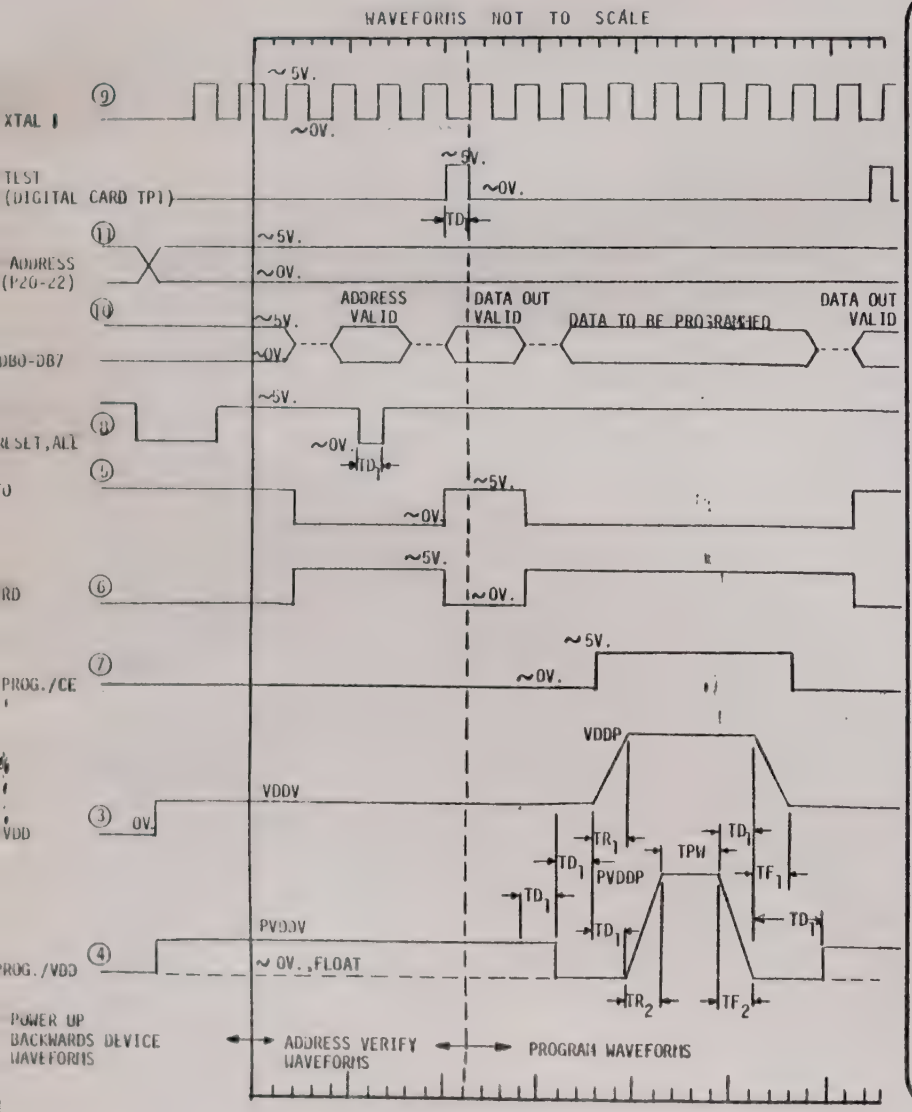
Please send all parts orders to:

DATA I/O CORPORATION
P O Box 308
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

DATE	SYM	REVISION RECORD	DR.	CK
4-25-78	A	RELEASE	PW	
8-8	B	ECN #2407		
2-79	-	ECN #2594	FS	



NOTES

DIGITAL CARD JUMPERS

JP1 = 1 PULSE REJECT = POS. A
JP1 = NO REJECT = POS. B
JP2 = SHORT

WAVEFORM VARIABLES

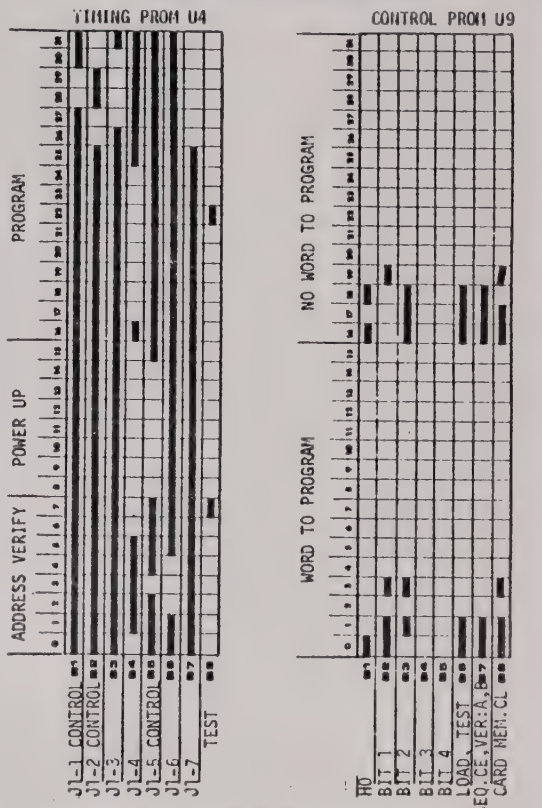
CLK RATE (FAST), ADJUST R5 FOR TD
CLK RATE (SLOW), ADJUST R6 FOR TPW
TD_1 = 200 ± 20 us
TPW = 55 ± 5 ms
TR_2=TF_2 = .5 TO 2 us
XTAL 1 PERIOD = 750 ± 50 ns Adjust R1
VCC = 5.00 ± 0.20 V.
VDDV = 5.00 ± 0.20 V.
VDDP = 24.3 ± 0.2 V.
PVDDV = VDDV(8755A) = 0 V. (8755)
= FLOAT (8741/48)
PVDDP = VDDP
VEAH = 23.0 ± 0.5 V.
VEAL = ~1 V.
TR_1 = TF_1 = 10-100 us

○ These waveforms correspond to call-outs on the Calibration Chart. Switch S2 and S3 of the Universal Calibrator to indicated positions to obtain waveforms. Refer to Performance Check section of manual for detailed steps.

For calibration, the card set polarity defaults to VOH.

TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)



DATA I/O ISSAQUAH, WASH.

TIMING DIAGRAM

DRAWN BY P. WALTER

APPROVED BY

TITLE
INTEL UPI-41, HCS-48

DATE 4-25-78

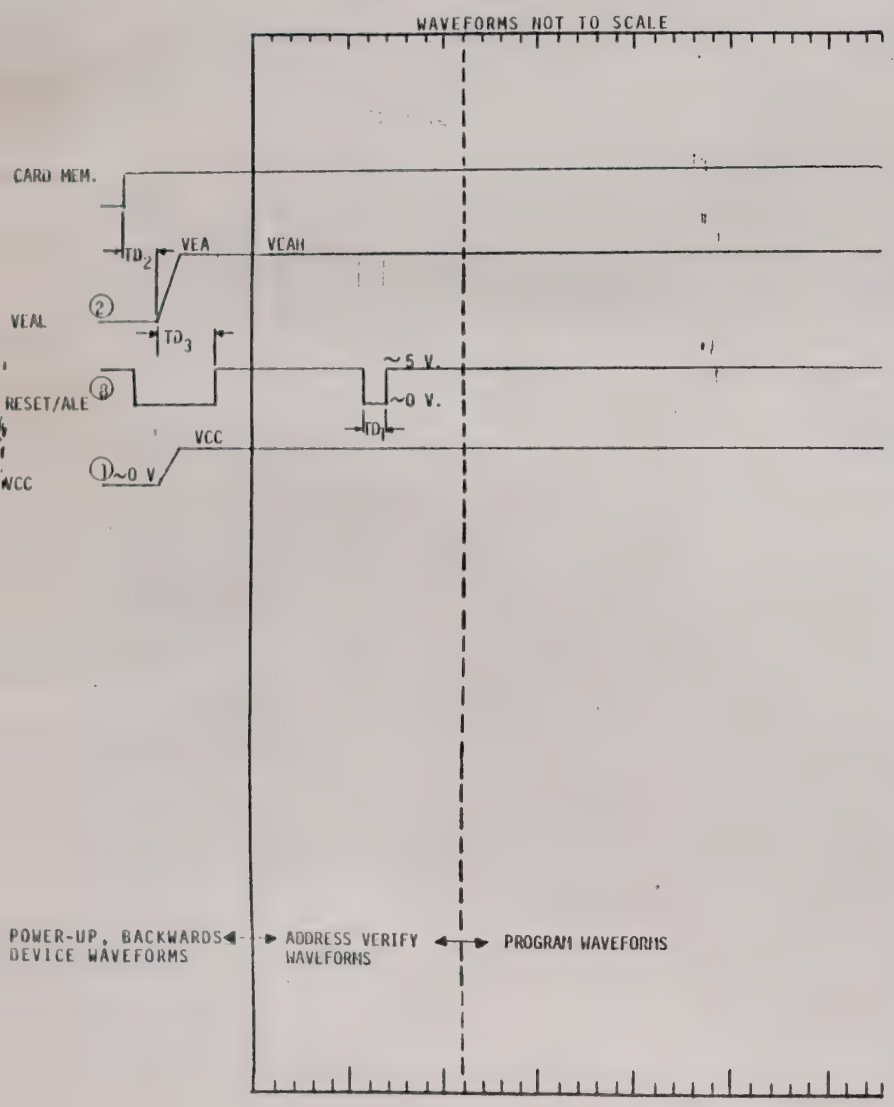
DRAWING NUMBER 007-1417

Sheet 1 of 2

DATE	SYM	REVISION RECORD	DR	CK
		See Sheet 1 of 2		

(WAVEFORMS CONTINUED)

WAVEFORMS NOT TO SCALE



NOTES

WAVEFORM VARIABLES

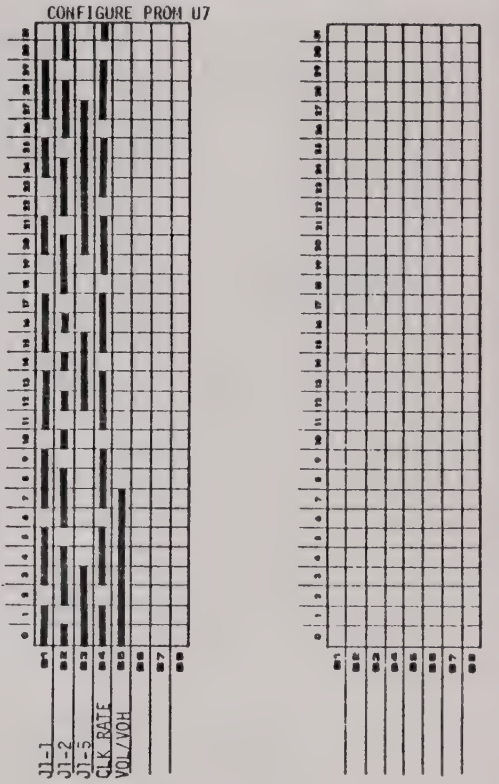
VCC = 5 ± .2 V.
VEAH = 23.0 ± .5 V.
VEAL = ~1 V.
TD_1 = 200 us ± 20 us
TD_2 = ~3 ms
TD_3 = ~1.5 ms

For calibration, the card set polarity defaults to VOH.

TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)

CONFIGURE PROM U7



DATA I/O ISSAQUAH, WASH.

TIMING DIAGRAM

DRAWN BY P. WALTER

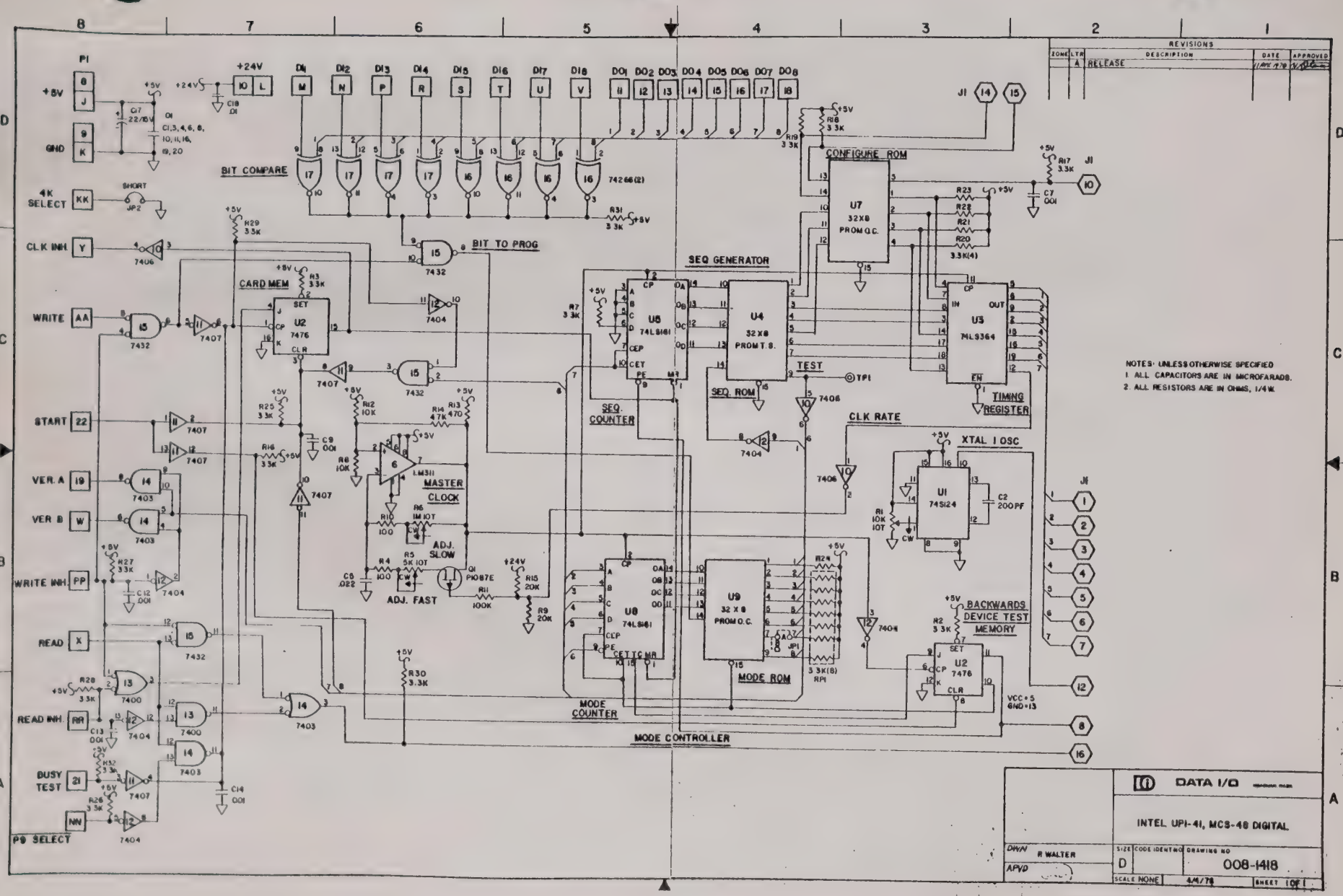
APPROVED BY

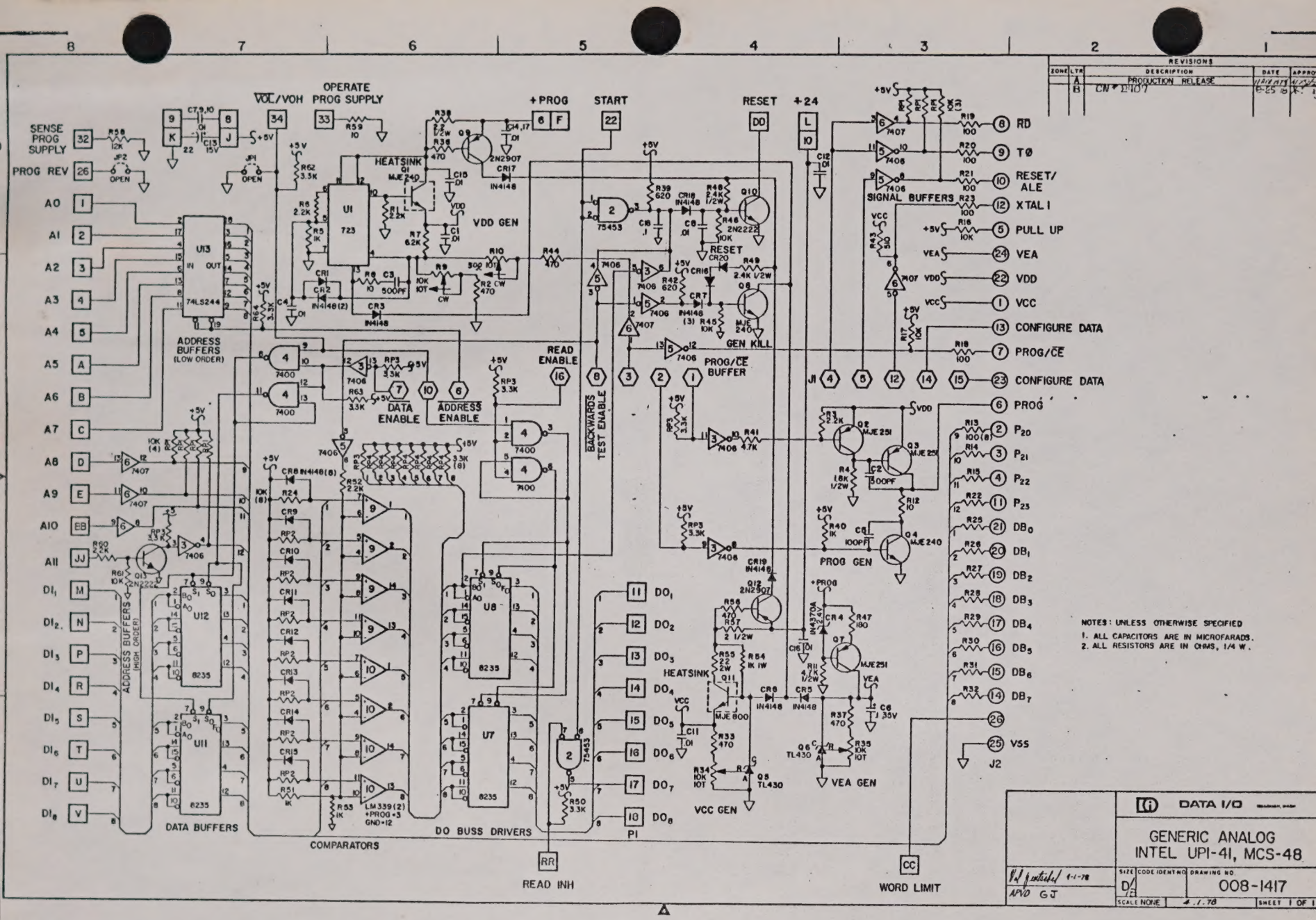
TITLE INTEL UPI-41, MCS-48

DATE 4-25-78

DRAWING NUMBER 007-1417

Sheet 2 of 2


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A RELEASE
P1
+8V
GND
4K SELECT
SHORT
JP2
+24V
BIT COMPARE
BIT TO PROG
CLK INH
WRITE
WRITE INH
READ
READ INH
BUSY TEST
P9 SELECT
START
VER A
VER B
CARD MEM
SEQ GENERATOR
SEQ. COUNTER
SEQ. ROM
TEST
TIMING REGISTER
CLK RATE
XTAL I OSC
MASTER CLOCK
ADJ. SLOW
ADJ. FAST
CONFIGURE ROM
MODE COUNTER
MODE ROM
MODE CONTROLLER
BACKWARDS DEVICE TEST MEMORY
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS, 1/4W.
DATA I/O
INTEL UPI-41, MCS-48 DIGITAL
DWN R WALTER
APVD
SIZE D
DRAWING NO 008-1418
SCALE NONE
SHEET 1 OF 1


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPRO
A | PRODUCTION RELEASE
B | CN # 2107
OPERATE
VOL/VOH PROG SUPPLY
+PROG
START
RESET
+24
SENSE PROG SUPPLY
PROG REV
HEATSINK
VDD GEN
RESET
GEN KILL
PROG/CE BUFFER
SIGNAL BUFFERS
RD
TØ
RESET/ ALE
XTAL I
PULL UP
VEA
VDD
VCC
CONFIGURE DATA
PROG/CE
CONFIGURE DATA
PROG
P20
P21
P22
P23
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
VSS
J2
ADDRESS BUFFERS (LOW ORDER)
ADDRESS BUFFERS (HIGH ORDER)
DATA BUFFERS
DATA ENABLE
ADDRESS ENABLE
READ ENABLE
BACKWARDS TEST ENABLE
COMPARATORS
DO BUSS DRIVERS
PROG GEN
VCC GEN
VEA GEN
READ INH
WORD LIMIT
PI
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS, 1/4 W.
DATA I/O
GENERIC ANALOG
INTEL UPI-41, MCS-48
SIZE D
DRAWING NO. 008-1417
SCALE NONE
4.1.78
SHEET 1 OF 1

DUO-TANG
1258
MADE IN U.S.A.